Amendments to the Claims

Please amend Claims 1, 19, 23, 27, 44, 48, 51, 59 and 63. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (currently amended) A data transmitter comprising:

a data input;

plural delay elements that apply different delays to the data input ~~in parallel~~ to provide plural delayed data signals; and

a data output that combines the delayed data signals, a rise or fall transition time of the data output being determined by different delays applied to the data input, wherein the rise or fall transition time of the data output signal is greater than the rise or fall transition time of the data input.

2. (original) A data transmitter as claimed in claim 1 wherein plural of the delay elements are parallel delay elements connected in series with a common delay element.

3. (original) A data transmitter as claimed in claim 1 wherein a clock signal is applied to the delay elements and different delays are applied to the data input by clocking the data input with different delayed clock signals.

4. (original) A data transmitter as claimed in claim 3 wherein the delayed clock signals sequence the data input into plural driver circuits.

5. (original) A data transmitter as claimed in claim 4 wherein each delay element comprises CMOS inverters.

6. (original) A data transmitter as claimed in claim 5 wherein delay of the delay elements is determined by load capacitance.

7. (original) A data transmitter as claimed in claim 1 wherein the data input is applied in parallel to the delay elements.

8. (original) A data transmitter as claimed in claim 7 wherein the delayed data signals are applied to plural driver circuits.

9. (original) A data transmitter as claimed in claim 8 wherein each delay element comprises CMOS inverters.

10. (original) A data transmitter as claimed in claim 9 wherein delay of the delay elements is determined by load capacitance.

11. (original) A data transmitter as claimed in claim 1 wherein the transition time of the data output is proportional to bit time.

12. (original) A data transmitter as claimed in claim 1 wherein supply voltage to the delay elements is controlled to control delay of the delay elements.

13. (original) A data transmitter as claimed in claim 12 further comprising a circuit to control the supply voltage to the delay elements, the circuit comprising:

first and second delay elements, each receiving a common clock signal; and

a phase comparator which compares outputs of the first and second delay elements and controls a supply voltage applied to the first and second delay elements to control phase difference of the outputs.

14. (original) A data transmitter as claimed in claim 13 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

15. (original) A data transmitter as claimed in claim 12 wherein the supply voltage is varied to compensate for environmental changes in delay.

16. (original) A data transmitter as claimed in claim 1 further comprising a circuit to control the supply voltage to the delay elements, the circuit comprising:

first and second delay elements, each receiving a common clock signal; and

a phase comparator which compares outputs of the first and second delay elements and controls a supply voltage applied to the first and second delay elements to control phase difference of the outputs.

17. (original) A data transmitter as claimed in claim 16 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

18. (previously presented) A data transmitter comprising:

a data input;

a bit clock; and

rise or fall transition time control receiving the data input and providing a controlled data signal, the transition time control controlling the transition time of the controlled data signal to be proportional to bit time of the bit clock.

19. (currently amended) A data transmitter as claimed in claim 18 wherein a clock signal is applied to [[the]] delay elements and different delays are applied to the data input by clocking the data input with different delayed clock signals.

20. (original) A data transmitter as claimed in claim 19 wherein the delayed clock signals sequence the data input into plural driver circuits.

21. (original) A data transmitter as claimed in claim 20 wherein each delay element comprises CMOS inverters.

22. (original) A data transmitter as claimed in claim 21 wherein delay of the delay elements is determined by load capacitance.

23. (currently amended) A data transmitter as claimed in claim 18 wherein the data input is applied to [[the]] parallel delay elements.

24. (original) A data transmitter as claimed in claim 23 wherein the delay data signals are applied to plural driver circuits.

25. (original) A data transmitter as claimed in claim 24 wherein each delay element comprises CMOS inverters.

26. (original) A data transmitter as claimed in claim 25 wherein delay of the delay elements is determined by load capacitance.

27. (currently amended) A data transmitter as claimed in claim [[18]] 19 wherein supply voltage to the delay elements is controlled to control delay of the delay elements.

28. (original) A data transmitter as claimed in claim 27 further comprising a circuit to control the supply voltage to the delay elements, the circuit comprising:

first and second delay elements, each receiving a common clock signal; and

a phase comparator which compares outputs of the first and second delay elements and controls a supply voltage applied to the first and second delay elements to control phase difference of the outputs.

29. (original) A data transmitter as claimed in claim 28 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

30. (original) A data transmitter as claimed in claim 27 wherein the supply voltage is varied to compensate for environmental changes in delay.

31. (original) A data transmitter as claimed in claim 18 further comprising a circuit to control the supply voltage to the delay elements, the circuit comprising:

first and second delay elements, each receiving a common clock signal; and

a phase comparator which compares outputs of the first and second delay elements and controls a supply voltage applied to the first and second delay elements to control phase difference of the outputs.

32. (original) A data transmitter as claimed in claim 31 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

33. (previously presented) A method of transmitting data comprising:

applying different delays to a data input to provide plural delayed data signals; and

combining the plural delayed data signals to provide a data output having a rise or fall transition time determined by different delays applied to the data input, wherein the rise or fall transition time of the data output signal is greater than the rise or fall transition time of the data input.

34. (original) A method as claimed in claim 33 wherein the different delays are obtained by applying a first delay to the data input and further delaying in parallel delay elements.

35. (original) A method as claimed in claim 34 wherein a clock signal is applied to the delay elements and different delays are applied to the data input by clocking the data input with different delayed clock signals.

36. (original) A method as claimed in claim 35 wherein the delayed clock signals sequence the data input into plural driver circuits.

37. (original) A method as claimed in claim 36 wherein each delay is obtained in CMOS inverters.

38. (original) A method as claimed in claim 37 wherein delay of the delay elements is determined by load capacitance.

39. (original) A method as claimed in claim 34 wherein the data input is applied in parallel to the delay elements.

40. (original) A method as claimed in claim 39 wherein the delay data signals are applied to plural driver circuits.

41. (original) A method as claimed in claim 40 wherein each delay element comprises CMOS inverters.

42. (original) A method as claimed in claim 41 wherein delay of the delay elements is determined by load capacitance.

43. (original) A method as claimed in claim 33 wherein the transition time of the data output is proportional to bit time.

44. (currently amended) A method as claimed in claim [[33]] 34 further comprising controlling supply voltage to the delay elements to control delay of the delay elements.

45. (original) A method as claimed in claim 44 wherein the supply voltage to the delay elements is controlled by:

applying a common clock signal to first and second delay elements; and

comparing outputs of the first and second delay elements and controlling the supply voltage applied to the first and second delay elements to control phase difference of the output.

46. (original) A method as claimed in claim 45 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal is 1/n bit rate.

47. (original) A method as claimed in claim 44 wherein the supply voltage is varied to compensate for environmental changes in delay.

48. (currently amended) A method as claimed in claim [[33]] 34 wherein the supply voltage to the delay elements is controlled by:

applying a common clock signal to first and second delay elements; and

comparing outputs of the first and second delay elements and controlling the supply voltage applied to the first and second delay elements to control phase difference of the outputs.

49. (original) A method as claimed in claim 48 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

50. (previously presented) A method of transmitting data comprising:

providing a bit clock;

receiving a data input; and

converting the data input to a controlled data signal having a controlled rise or fall transition time, the rise or fall transition time of the controlled data signal being proportional to bit time of the bit clock.

51. (currently amended) A method as claimed in claim [[18]] 50 wherein a clock signal is applied to [[the]] delay elements and different delays are applied to the data input by clocking the data input with different delayed clock signals.

52. (original) A method as claimed in claim 51 wherein the delayed clock signals sequence the data input into plural driver circuits.

53. (original) A method as claimed in claim 52 wherein each delay element comprises CMOS inverters.

54. (original) A method as claimed in claim 53 wherein delay of the delay elements is determined by load capacitance.

55. (original) A method as claimed in claim 50 wherein the data input is applied in parallel to delay elements.

56. (original) A method as claimed in claim 55 wherein the delay data signals are applied to plural driver circuits.

57. (original) A method as claimed in claim 56 wherein each delay element comprises CMOS inverters.

58. (original) A method as claimed in claim 57 wherein delay of the delay elements is determined by load capacitance.

59. (currently amended) A method as claimed in claim [[50]] 51 further comprising controlling supply voltage to the delay elements to control delay of the delay elements.

60. (original) A method as claimed in claim 59 wherein the supply voltage to the delay elements is controlled by:

applying a common clock signal to first and second delay elements; and

comparing outputs of the first and second delay elements and controlling the supply voltage applied to the first and second delay elements to control phase difference of the output.

61. (original) A method as claimed in claim 60 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal frequency is 1/n times bit rate.

62. (original) A method as claimed in claim 59 wherein the supply voltage is varied to compensate for environmental changes in delay.

63. (currently amended) A method as claimed in claim [[50]] 51 wherein the supply voltage to the delay elements is controlled by:

applying a common clock signal to first and second delay elements; and

comparing outputs of the first and second delay elements and controlling the supply voltage applied to the first and second delay elements to control phase difference of the outputs.

64. (original) A method as claimed in claim 63 wherein each of the first and second delay elements comprises a sequence of n elements and the clock signal is 1/n times bit rate.

65. (previously presented) A data transmitter comprising:

a data input;

plural delay means for applying different delays to the data input to provide plural delayed data signals; and

data output means for combining the delayed data signals into a data output having a rise or fall transition time determined by different delays applied to the data input, wherein the rise or fall transition time of the data output signal is greater than the rise or fall transition time of the data input.

66. (previously presented) A data transmitter comprising:

data input;

a bit clock; and

rise or fall transition time control means for providing a controlled data signal from the data input, the rise or fall transition time of the controlled data signal being proportional to bit time of the bit clock.